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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/965,286	Gomi et al.
Examiner	**Art Unit**
ORI NADAV	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 5, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 3, 4, 6, and 20-29* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3, 4, 6, and 20-29* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 27-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of each impurity concentration of the high voltage diffusion layer being located between the high voltage peak impurity concentration (HVPIC) and the datum, as recited in claim 27, is unclear as to the location of the each impurity concentration of the high voltage diffusion layer, since the impurity concentration is located between a concentration (HVPIC) and a datum.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6, 21, 23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. (4,379,726) or Watanabe et al. (4,258,379). Kumamaru et al. teach in figure 10 a semiconductor device having a first vertical bipolar transistor 15 and a second vertical type transistor 13 having a breakdown voltage that is higher than that of the first vertical type transistor, formed on a semiconductor substrate comprising a first conductivity type silicon substrate 1, 5 defining a datum bottom surface, an epitaxial layer 11 formed on the substrate above the datum surface, a first embedded diffusion layer 14 formed as part of a first vertical bipolar transistor 15 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 13 (figure 8) formed as part of a second vertical type transistor 13 directly on the substrate in a second upper part of the substrate and within a lower part of the epitaxial layer (column 3, lines 23-26), wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer, and having opposite conductivity type as that of the substrate and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer 14 and is approximately equal to or higher than the impurity concentration of the epitaxial layer (column 3, lines 16 and 27-28), wherein peak positions of impurity concentrations of the first and second embedded diffusion layers

reside at first and second distances from the datum surface of the substrate, such that the first distance is greater than the second distance.

Although figure 10 of Kumamaru et al. does not depict a second embedded diffusion layer 13 being formed within a lower part of the epitaxial layer 11, Kumamaru et al. teach in column 3, lines 23-26, that the second embedded diffusion layer 13 is formed within a lower part of the epitaxial layer. Therefore, the claimed structure is considered to be at least obvious over Kumamaru et al.'s structure.

Watanabe et al. teach in figure 8 a semiconductor device having a first vertical bipolar transistor 101 and a second vertical type transistor 201 having a breakdown voltage that is higher than that of the first vertical type transistor, comprising a first conductivity type silicon substrate 1 defining a datum bottom surface, an epitaxial layer 3 formed on the substrate above the datum surface, a first embedded diffusion layer 21 formed as part of a first vertical bipolar transistor 101 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 22" formed as part of a second vertical type transistor directly on the substrate in a second upper part of the substrate and within a lower part of the epitaxial layer, wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer, and having opposite conductivity type as that of the substrate and having an

impurity concentration less than the impurity concentration of the first embedded diffusion layer and is approximately equal to or higher than the impurity concentration of the epitaxial layer (figure 9), wherein peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, such that the first distance is greater than the second distance.

Although figure 8 of Watanabe et al. does not clearly depict a second embedded diffusion layer 22" being formed within a lower part of the epitaxial layer 3, figure 9 clearly shows a second embedded diffusion layer 22" being formed within a lower part of the epitaxial layer 3. Therefore, the claimed structure is considered to be at least obvious over Watanabe et al.'s structure.

Regarding claim 3, Kumamaru et al. teach a bottom of the first embedded diffusion layer 14 being formed at a smaller distance from the datum surface (the interface between layers 11 and 5) than the midpoint of the second embedded diffusion layer. Note that the broad recitation of the claim does not require the datum surface to be the bottom surface of the substrate.

Watanabe et al. teach in figure 9 a bottom of the first embedded diffusion layer 21 being formed at a smaller distance from the datum surface than the midpoint of the second embedded diffusion layer 22".

Regarding claim 4, although figure 10 of Kumamaru et al. does not depict a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer, it is well known in the art that diffused areas have concentration that follows natural distribution curve, of which official notice may be taken (See Watanabe et al.' figure 9, graph 22"). In the alternative, the second embedded diffusion layer can comprise layers 13 and 12. Thus, the second embedded diffusion layer has impurity concentration portions that are equal and greater than that of the epitaxial layer, as claimed.

Watanabe et al. teach in figure 9 a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer.

Regarding claim 6, Kumamaru et al. and Watanabe et al. teach a datum surface being the bottom surface of the substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Kumamaru et al. and Watanabe et al.s' devices, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 23, Kumamaru et al. and Watanabe et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type

bipolar transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Regarding claims 25-26, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

5. Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al.

Kumamaru et al. teach substantially the entire claimed structure, as applied to claim 1 above, including first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers to define first and second epitaxial thicknesses, respectively, wherein the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

6. Claim 22, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. or Watanabe et al. in view of Admitted Prior Art (APA).

Kumamaru et al. and Watanabe et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is

approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface.

APA teaches in figures 3 and 4 a peak position of an impurity concentration of the second embedded diffusion layer residing at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the peak position of an impurity concentration of the second embedded diffusion layer at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface in Kumamaru et al. and Watanabe et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

7. Claims 27 and 29, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. in view of Watanabe et al.

Kumamaru et al. teach in figure 8 a semiconductor device comprising a substrate 1 having a first surface that defines a datum, a high speed diffusion layer 14 comprising a first surface disposed above the datum at a first height, a high voltage diffusion layer 13

(figure 8) comprising a first surface disposed at a second height, wherein the second height is substantially at the datum, a high speed base layer 21 comprising a lower surface that faces the first surface of the high speed diffusion layer and is disposed at a first speed height from the datum; a high voltage base layer 17 comprising a lower surface that faces the second surface of the high voltage diffusion layer and is disposed at a first voltage height from the datum, wherein the first speed height of the high speed base layer is equal to the first voltage height of the high voltage base layer; an epitaxial layer 11, wherein the epitaxial layer is disposed between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer, and wherein only the epitaxial layer is disposed between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer, wherein the high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value and wherein the high voltage (HV) diffusion layer comprises a peak impurity concentration (HVPIC) value, such that the high voltage peak impurity concentration (HVPIC) value is less than the high speed peak impurity concentration (HSPIC) value, and wherein each impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum can be higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer.

Kumamaru et al. do not state the precise impurity concentration of the high voltage diffusion layer.

Watanabe et al. teach in figures 4 and 9 each impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum is higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to adjust the impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum to be higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer in Kumamaru et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization to find the optimum working characteristics of the device.

Regarding claim 29, Kumamaru et al. teach in figure 8 an epitaxial layer between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer defines a thin collector layer, wherein the epitaxial layer between the first surface of the high voltage diffusion layer and the lower surface of the high voltage

base layer defines a thick collector layer, wherein the thick collector layer is thicker than the thin collector layer.

8. Claim 28, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. and Watanabe et al., as applied to claim 27 above, and further in view of Admitted Prior Art (APA).
Kumamaru et al. and Watanabe et al. teach substantially the entire claimed structure, as applied to claim 27 above, including a high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value that is disposed at distance Yhspic below the datum, wherein the high voltage (HV) diffusion layer comprises a peak impurity concentration (HVPIC) value that is disposed at distance Yhvpic below the datum.
Kumamaru et al. and Watanabe et al. do not teach Yhvpic > Yhspic
APA teaches in figures 3 and 4 Yhvpic > Yhspic.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Yhvpic > Yhspic in Kumamaru et al. and Watanabe et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Response to Arguments

9. Applicant argues on pages 7-8 that figure 8 of Kumamaru et al. can not be combined with figure 10.

The examiner does not use figure 8 to reject the claimed invention. Layer 13 of figure 8 was cited as courtesy and convenience to applicant to identify which layer of figure 10 was cited in the rejection.

10. Applicant argues on page 7 that converting substrate 5 into element 13 does not mean that element 13 is formed directly on the substrate.

It is unclear how converting a section of a substrate into an element would not result in the element being located directly on the substrate.

11. Applicant's arguments on pages 9-11 were adequately addressed in previous office actions.

12. The rest of applicant's arguments on pages 12-13 have been considered but are moot in view of the new ground(s) of rejection.